ADF7023-J Silicon Rev. 2.2 PCN Technical Content

Rev. 0

Temperature Sensor

The formula for calculating the die temperature from the ADC readback of the temperature sensor has changed. The new formula is given below.

Temperature (°C) = 0.9474 x (ADC_READBACK[7:0] – CalibrationValue[7:0]) + $T_{Calibration}$

The CalibrationValue[7:0] is determined via an ADC readback at a temperature of $T_{Calibration}$

Monotonicity of Transmitter Output Power versus PA_LEVEL setting

On previous versions of the ADF7023-J, when using the single ended PA, the increase in transmitter output power with increasing PA_LEVEL setting was non-monotonic at PA_LEVEL = 58. This has been corrected on the current silicon. Refer to the Typical Performance Characteristics section of ADF7023-J datasheet revision A for the updated output power versus PA_LEVEL setting characteristic. Transmitter output power at all other values of PA_LEVEL are unaffected.

Interrupt Pin Behavior in PHY_SLEEP

When in PHY_SLEEP the IRQ_GP3 pin is now held at logic low on this version of the ADF7023-J. On previous versions it was in a high impedance state.

Image Rejection

The values to be written to IMAGE_REJECT_CAL_PHASE (Address 0x118) and IMAGE_REJECT_CAL_AMPLITUDE (Address 0x119) to achieve the specified uncalibrated image attenuation values given in the ADF7023-J datasheet have changed on this revision of the ADF7023-J.

To achieve the specified uncalibrated image attenuation at 915 MHz, set IMAGE_REJECT_CAL_AMPLITUDE = 0x07 and IMAGE_REJECT_CAL_PHASE = 0x16

Interrupt Timing Upon Entering PHY_TX State

Following the issue of CMD_PHY_TX, the latency from the interrupt indicating the part is in PHY_TX to data transmission has been reduced on this version of the ADF7023-J, data transmission will begin 1.5 x T_{bit} + 2.3µs following the interrupt. T_{bit} is the time taken to transmit a bit at the selected datarate. The PA ramp will start 3.4µs after the interrupt.

External PA and LNA Control Signals

When external PA and LNA control signals are enabled via register 0x11A[0], the configuration of these signals are now set via register 0x139[7] rather than via 0x11B[7] as on previous versions of the ADF7023. This functionality is described in Table 1.

Table 1. 0x139: BB_Testmodes

Bit	Name	R/W	Description	
[7]	EXT_PA_LNA_CONFIG	R/W	**EXT_PA_LNA_CONFIG**	**Description**
			0	External PA signal on XOSC32KP_GP5_ATB1 and external LNA signal on XOSC32KN_ATB2 (V_{DD} logic outputs)
			1	External PA signal on ADCIN_ATB3 and external LNA signal on ATB4 (1.8 V logic outputs)

Smart Wake Mode RSSI Prequalification and CMD_GET_RSSI

When using RSSI prequalification in Smart Wake Mode or when using CMD_GET_RSSI, the time between powering up the receiver blocks and taking a RSSI measurement is now programmable via register 0x138. For more information refer to the ADF7023-J datasheet revision A. The operation of RSSI method 1 and RSSI method 3 is unaffected by this change.

BBRAM Registers 0x138 to 0x13D

BBRAM registers from 0x138 to 0x13D now have new functionality. They may no longer be used for address matching or for static register fixes. The new functionality of these registers is described in the ADF7023-J datasheet revision A.

Downloadable Firmware Modules

If it is desired to use the Image Rejection Calibration or Reed Solomon Coding and AES Encryption/Decryption firmware modules, it is necessary to use the module versions consistent with this silicon revision of the ADF7023. The appropriate firmware modules are named as "rom_ram_7023_2_2_xxxx" and are available at:
ftp://ftp.analog.com/pub/RFL/FirmwareModules/ADF7023